

Claims

- [c1] 1. A thin film transistor array, comprising:
a substrate;
a plurality of scan lines disposed over the substrate;
a plurality of data lines disposed over the substrate,
wherein the substrate is defined into a plurality of pixel areas by the scan lines and the data lines;
a plurality of thin film transistor driven by the scan lines and the data lines, wherein each thin film transistor is disposed in one of the pixel areas correspondingly;
an etching stop layer disposed over the scan lines, wherein the etching stop layer has a plurality of openings; and
a plurality of pixel electrodes, each pixel electrode is disposed in one of the pixel areas and is electrically connected to one of the thin film transistors correspondingly, wherein a portion of each pixel electrode is coupled to one of the scan lines through one of the openings to form a storage capacitor.
- [c2] 2. The thin film transistor array of claim 1, further comprising a gate insulator disposed between the etching stop layer and the scan lines.

- [c3] 3. The thin film transistor array of claim 2, wherein the gate insulator has a plurality of recesses, and each recess is located under one of the openings of the etching stop layer.
- [c4] 4. The thin film transistor array of claim 2, further comprising a semiconductor layer disposed between the etching stop layer and the gate insulator.
- [c5] 5. The thin film transistor array of claim 2, further comprising a passivation layer disposed over the etching stop layer and the gate insulator, wherein the openings of the etching stop layer is exposed by the passivation.
- [c6] 6. The thin film transistor array of claim 1, wherein the etching stop layer comprises a plurality of stripe patterns, each stripe pattern is located above one of the scan lines correspondingly.
- [c7] 7. The thin film transistor array of claim 1, wherein the etching stop layer comprises a plurality of frame patterns, each frame pattern is located under one of the pixel electrodes correspondingly.
- [c8] 8. The thin film transistor array of claim 1, wherein a material of the pixel electrodes comprises ITO or IZO.
- [c9] 9. A thin film transistor array, comprising:

a substrate;
a plurality of scan lines disposed over the substrate;
a plurality of data lines disposed over the substrate,
wherein the substrate is defined into a plurality of pixel
areas by the scan lines and the data lines;
a plurality of thin film transistor driven by the scan lines
and the data lines, wherein each thin film transistor is
disposed in one of the pixel areas correspondingly;
a plurality of common lines disposed over the substrate,
wherein each common line is located between two adja-
cent scan lines;
an etching stop layer disposed over the common lines,
wherein the etching stop layer has a plurality of open-
ings; and
a plurality of pixel electrodes, each pixel electrode is
disposed in one of the pixel areas and is electrically con-
nected to one of the thin film transistors correspond-
ingly, wherein a portion of each pixel electrode is cou-
pled to one of the scan lines through one of the openings
to form a storage capacitor.

[c10] 10. The thin film transistor array of claim 9, further
comprising a gate insulator disposed between the etch-
ing stop layer and the common lines.

[c11] 11. The thin film transistor array of claim 10, wherein
the gate insulator has a plurality of recesses, and each

recess is located under one of the openings of the etching stop layer.

- [c12] 12. The thin film transistor array of claim 10, further comprising a semiconductor layer disposed between the etching stop layer and the gate insulator.
- [c13] 13. The thin film transistor array of claim 10, further comprising a passivation layer disposed over the etching stop layer and the gate insulator, wherein the openings of the etching stop layer is exposed by the passivation.
- [c14] 14. The thin film transistor array of claim 9, wherein the etching stop layer comprises a plurality of stripe patterns, each stripe pattern is located above one of the common lines correspondingly.
- [c15] 15. The thin film transistor array of claim 9, wherein the etching stop layer comprises a plurality of frame patterns, each frame pattern is located under one of the pixel electrodes correspondingly.
- [c16] 16. The thin film transistor array of claim 9, wherein a material of the pixel electrodes comprises ITO or IZO.
- [c17] 17. A fabricating method of a thin film transistor array, comprising:
forming a first patterned conductive layer over the sub-

strate;

forming a gate insulator and a semiconductor material layer over the substrate and the first patterned conductive layer sequentially;

forming an etching stop layer located above the first patterned conductive layer over a portion of the semiconductor material layer;

forming a second conductive material layer over the semiconductor material layer and the etching stop layer; patterning the second conductive material layer and the semiconductor material layer to simultaneously form a second patterned conductive layer and a plurality of semiconductor layers, which are located under the etching stop layer and the second patterned conductive layer;

forming a passivation layer over the substrate;

removing a portion of the passivation layer, which is located on the second patterned conductive layer, to form a plurality of contact windows, and removing a portion of the passivation layer, the etching stop layer and the semiconductor layers, which are located above the first patterned conductive layer, simultaneously; and

forming a plurality of pixel electrodes over the substrate, wherein each pixel electrode is electrically connected to the second patterned conductive layer through one of the contact windows, and a portion of each pixel elec-

trode is coupled to the first patterned conductive layer through one of the openings to form a storage capacitor.

- [c18] 18. The method of claim 17, wherein forming the first patterned conductive layer comprises:
forming a first conductive material layer over the substrate; and
patterning the first conductive material layer to form a plurality of scan lines and a plurality of gates connected with the scan lines.
- [c19] 19. The method of claim 18, wherein the etching stop layer is formed above the gates and the scan lines.
- [c20] 20. The method of claim 17, wherein forming the first patterned conductive layer comprises:
forming a first conductive material layer over the substrate; and
patterning the first conductive material layer to form a plurality of scan lines, a plurality of gates connected with the scan lines, and a plurality of common lines located between two adjacent scan lines.
- [c21] 21. The method of claim 20, wherein the etching stop layer is formed above the gates and the common lines.
- [c22] 22. The method of claim 17, further comprising:
removing partial thickness of the etching stop layer by

using the second patterned conductive layer as a mask during patterning the second conductive material layer and the semiconductor material layer.

[c23] 23. The method of claim 17, further comprising:
removing partial thickness of the gate insulator to form a plurality of recesses, which are located under the openings, when forming the contact windows.

[c24] 24. The method of claim 17, further comprising:
forming an ohmic contact layer over the semiconductor material layer and the etching stop layer before forming the second conductive material layer over the semiconductor material layer and the etching stop layer.